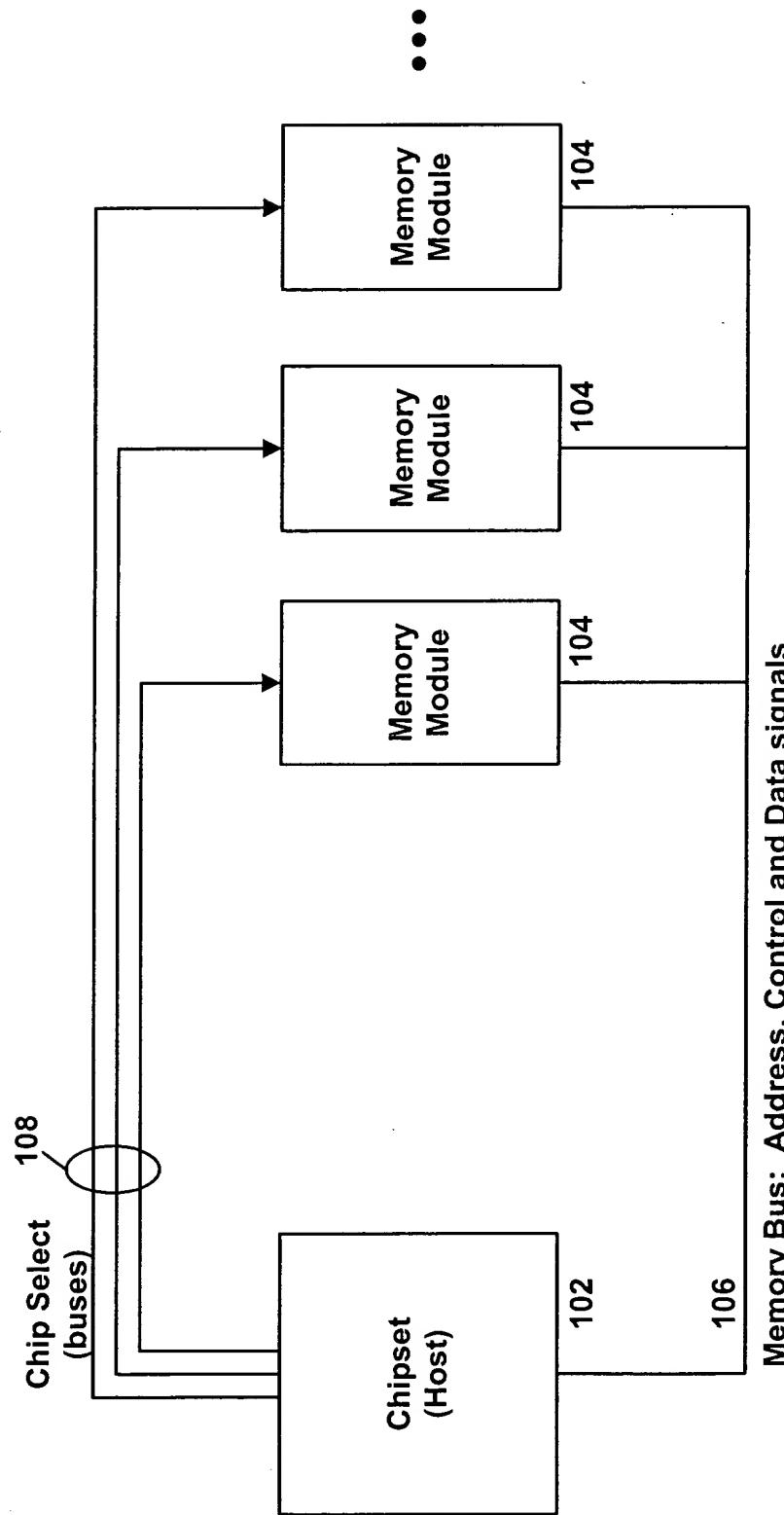




1/6

Memory Bus



Memory Bus: Address, Control and Data signals

*Figure 1
(Prior Art)*



Memory Bus Peripheral (FPGA) Operation

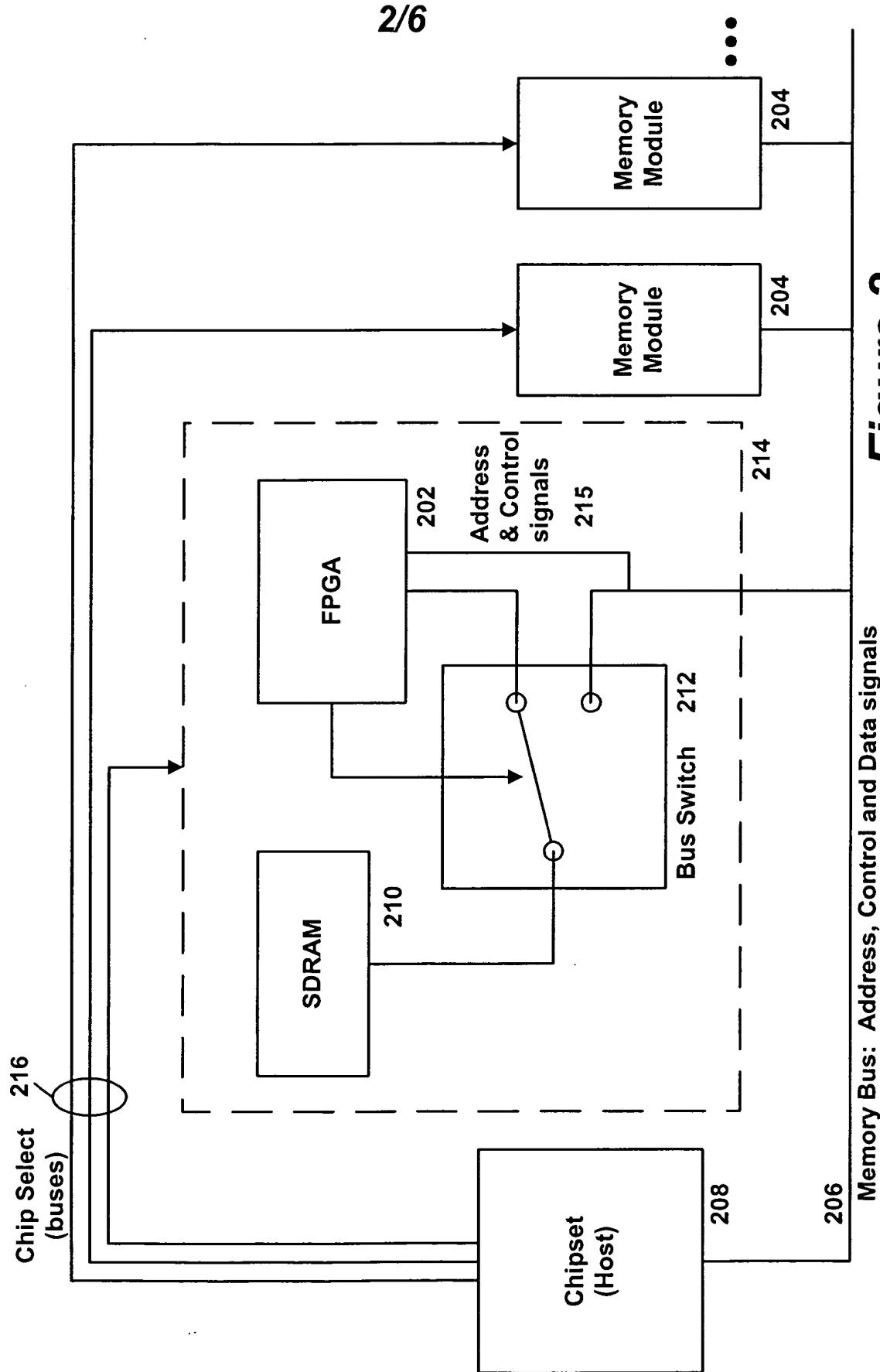


Figure 2

Memory Bus: Address, Control and Data signals



Operational Flowchart

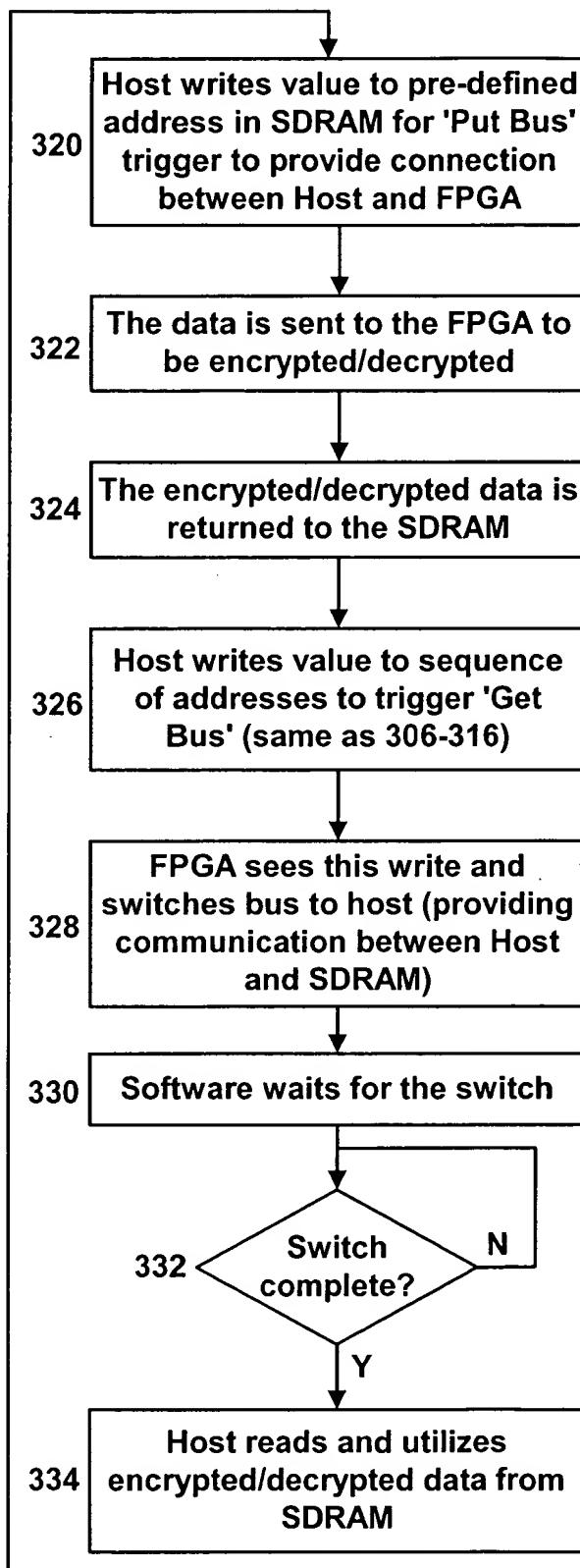
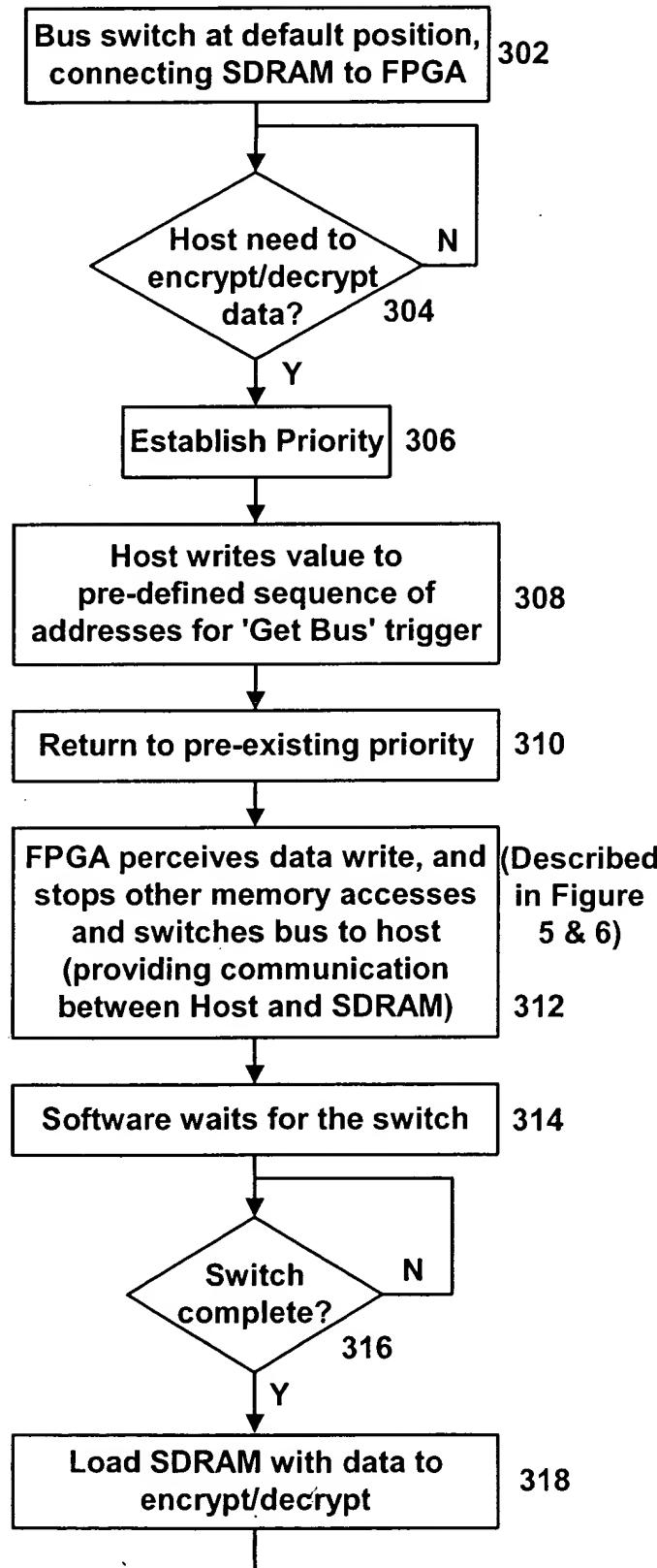


Figure 3



4/6

Example Memory Module Trigger Address Locations

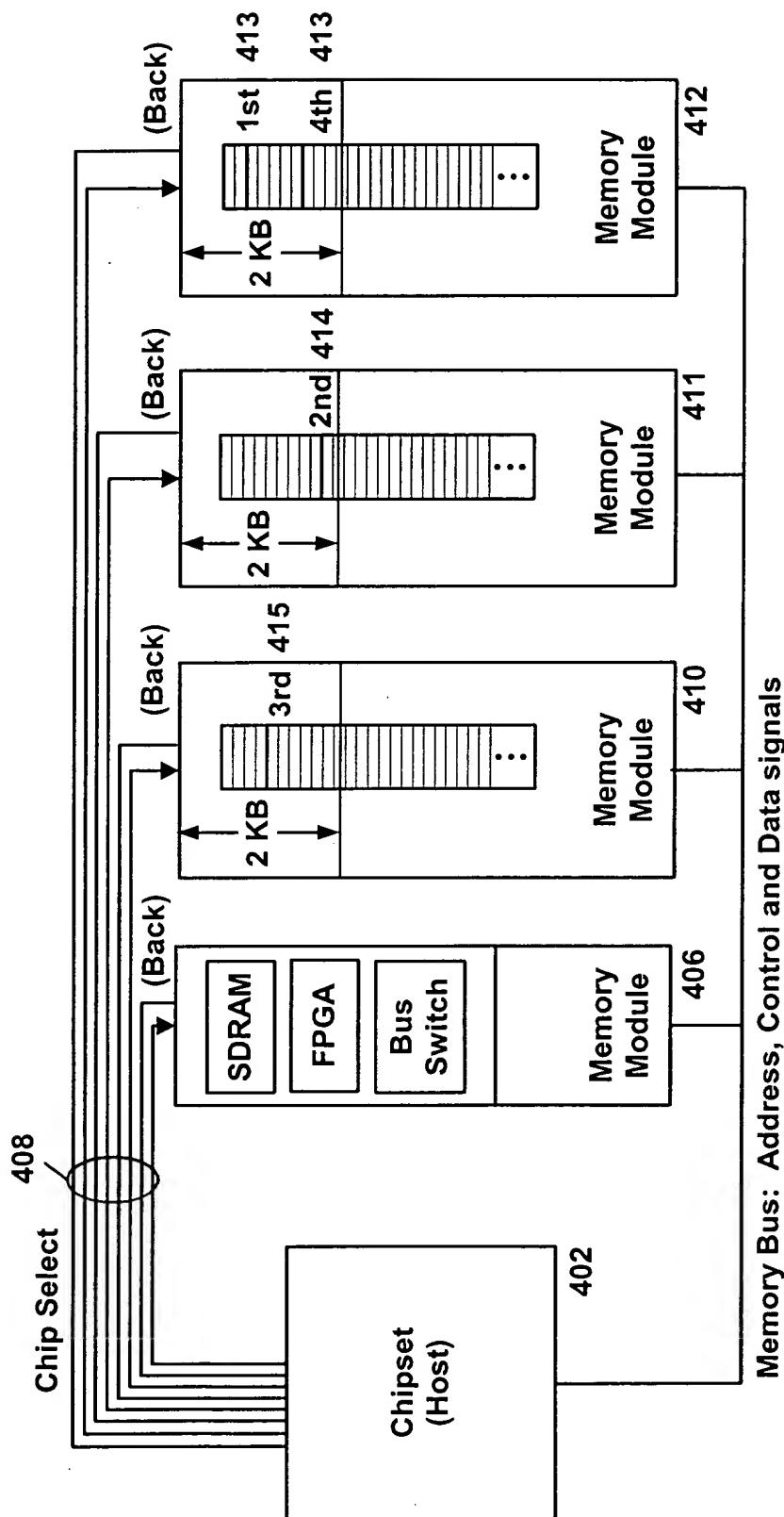


Figure 4

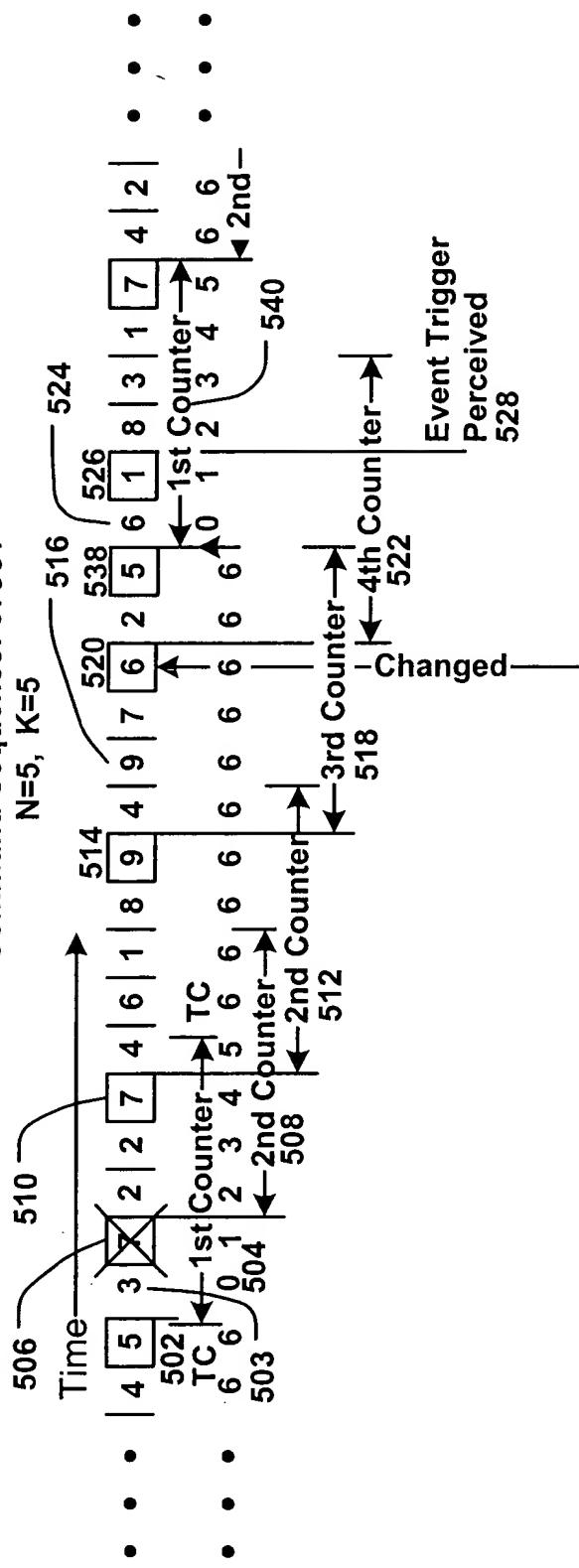
Memory Bus: Address, Control and Data signals



5/6

Time Chart Descriptive of Sequence Detection

Data Values Witnessed Over Time: ...45372274618949762561831742...
Command Sequence: 57961



Data Values Witnessed Over Time: ...45372274618949772561831742...
Command Sequence: 57061

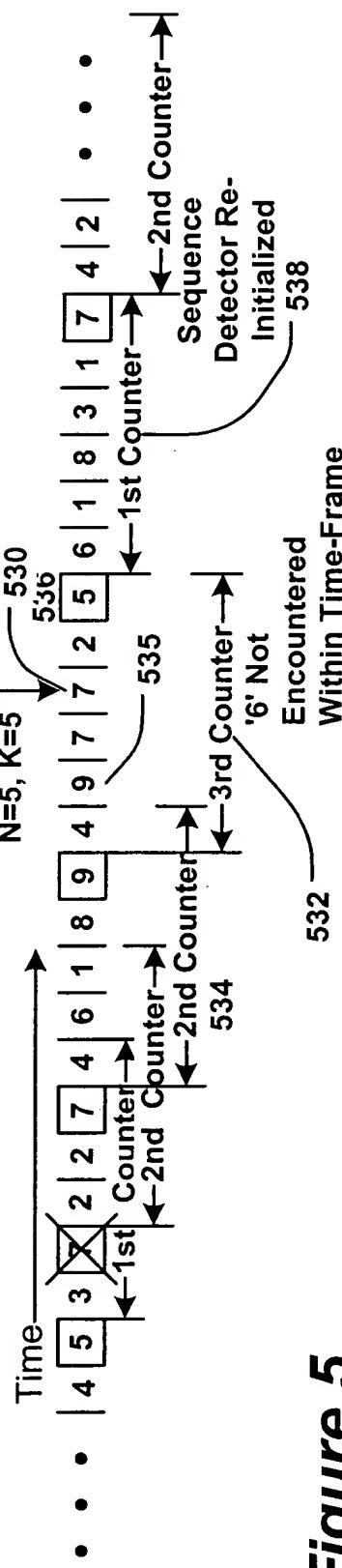


Figure 5

General Schematic of Data Value Sequence Detector

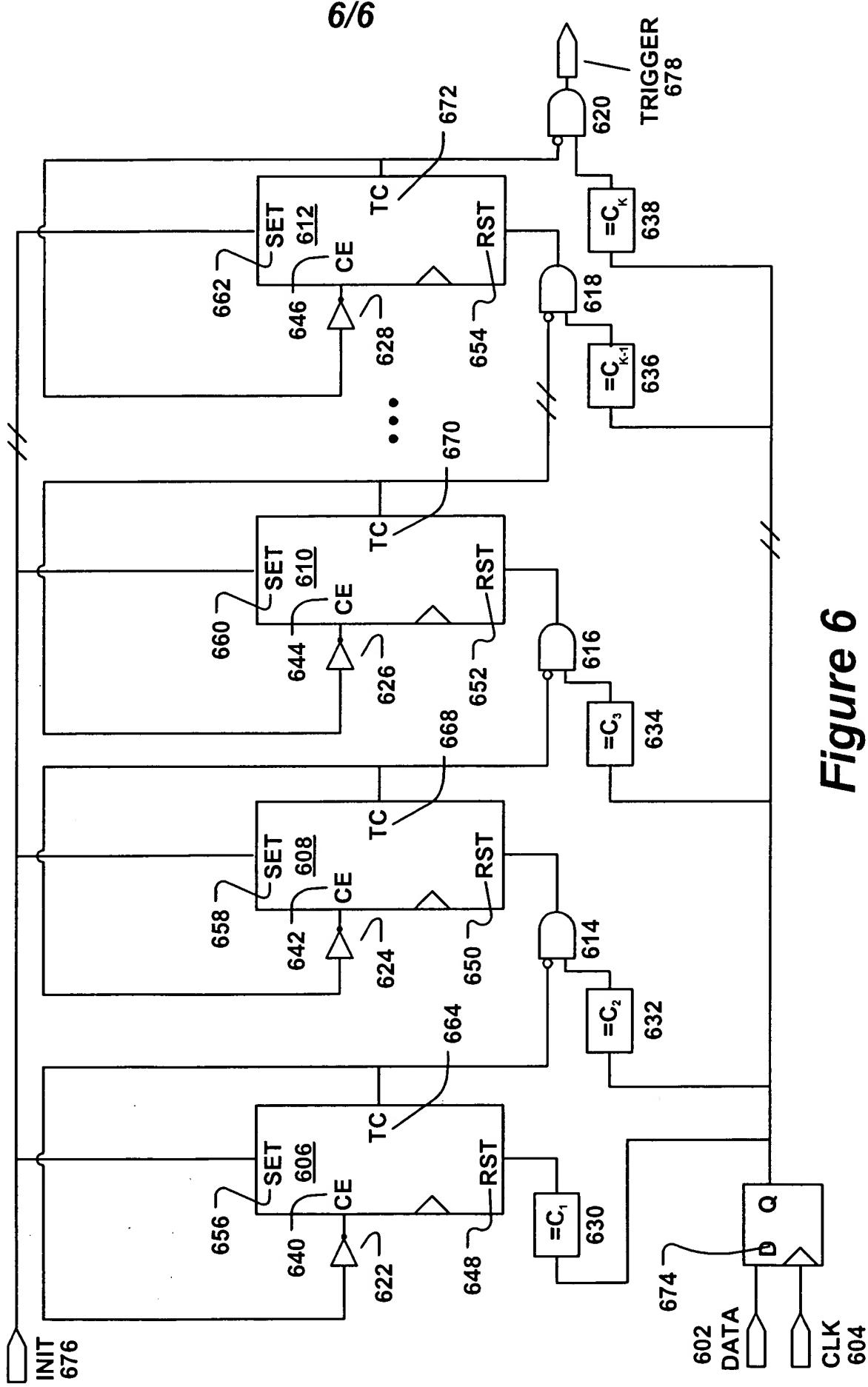


Figure 6

